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(54) Digital modulating method and digital modulating apparatus

Verfahren und Vorrichtung zur digitalen Modulation

Méthode et dispositif de modulation numérique

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- **PATENT ABSTRACTS OF JAPAN vol. 13, no. 537 (P-968), 30 November 1989; & JP-A-01220213**

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to digital modulating methods and digital modulating apparatus using the same, and particularly to a coding method in digital recording.

Description of the Background Art

Coding in digital recording means to convert a data word sequence with bit intervals of Tb into a codeword sequence with bit intervals of Ts according to a certain rule (a coding rule). Also, coding in which a data word sequence is divided for each information of m bits ($m \geqq 2$) and sequentially converted into a codeword of n bits ($n \geqq m$) is called block coding. The converted codeword sequence is further converted (modulated) into a recording pattern sequence (recording current form) according to the NRZL rule or the NRZI rule.

Now, coding according to the NRZL rule will be described. In the NRZL rule, a bit "0" corresponds to a certain level (e.g., a low level) and a bit "1" corresponds to another level (e.g., a high level) in a codeword sequence. If a minimum value of the number of continuing same bits in a codeword sequence is expressed as a parameter d (corresponding to a minimal runlength) and a maximum value thereof is expressed as a parameter k (corresponding to a maximal runlength), a minimum length between transitions Tmin and a maximal length between transitions Tmax are expressed as the following expressions, respectively.

$$Tmin = (m/n) \cdot d \cdot Tb \quad (1)$$

$$Tmax = (m/n) \cdot k \cdot Tb \quad (2)$$

Also, a ratio Tmin/Tb of the minimum length between transitions Tmin and the bit interval Tb of a data word sequence is referred to as a Density Ratio DR, which is expressed as the following expression.

$$DR = (m/n) \cdot d \quad (3)$$

In digital modulation, it is preferred that the minimum length between transitions Tmin is long and the maximal length between transitions Tmax is short. Also, a larger density ratio DR is more advantageous in high density recording. The relation among a data word sequence, a codeword sequence and a recording pattern sequence is shown in Fig. 15.

Accumulated charge obtained by, assigning charge +1 to a high level of a recording pattern sequence and assigning charge -1 to a low level, sequentially adding charges from the beginning of a recording pattern sequence is called DSV (Digital Sum Variation). That is to say, the DSV shows the difference between the numbers of bits "1" and bits "0" from the beginning to a certain bit in a recording pattern sequence. In the block coding, a total sum of charge in one codeword is called CDS (Code-word Digital Sum). That is to say, the CDS shows the difference between the numbers of bits "1" and bits "0" in one codeword.

Digital modulating methods according to the block coding method include the 8-10 modulating method in which a 8-bit data word is converted into a 10-bit codeword and then NRZ-or NRZI-modulated and recorded, the 8-14 modulating method in which a 8-bit data word is converted into a 14-bit codeword, NRZ or NRZI modulated and recorded, and so forth.

In order to precisely trace recording tracks in reproducing, tracking control is performed such as ATF (Automatic Track Finding), DTF (Dynamic Track Following) and so forth. It is necessary to record a pilot signal in each track of a recording medium for the tracking control. As a method of recording such a pilot signal, there is a recording method in which a pilot signal is superimposed upon digitally modulated data. This method, however, has problems, for example, that a reproduced signal is likely to undergo crosstalk disturbance due to a pilot signal in reproducing.

Accordingly, the 8-10 modulating method, the 12-15 modulating method and so forth are proposed in which control is performed so that DSV varies periodically in digital modulation and the periodical variation of DSV is used as a pilot signal. Such a 8-10 modulating method and a 12-15 modulating method are respectively described in "An Experimental Digital VCR with 40 mm Drum, Single Actuator and DCT-based Bit-rate Reduction" by S.M.C Borgers et al., IEEE Transactions on Consumer Electronics, Vol. 34, No. 3, August 1988, pp. 597-605, and in "A Study on the Servo Method for Home Use Digital VTR" by M. Nagasawa et al., Institute of Television Engineers of Japan (ITEJ) Technical Report Vol. 14, No. 41, VIR '90-43, Aug. 1990, pp. 1-6. In these modulating methods, tracking control is enabled with variation periods of DSV being different for each track. According to such modulating methods, a reproduced signal is prevented from undergoing crosstalk disturbance due to a pilot signal.

In the above-described 8-10 modulating method and 12-15 modulating method, the minimum length between transitions Tmin is 0.8Tb and the density ratio DR is 0.8. Thus, since the density ratio DR is smaller than 1, it is disadvantageous to high density recording.

EP-A-0 104 700 discloses a digital modulating method for converting an 8-bit data word sequence into a 16-bit codeword sequence whose d.c. content varies at a low frequency to provide an active tracking control. The method provides a minimum length between transitions Tmin of 1 Tb and a recording density DR of 1.

EP-A-0 319 101 discloses a digital modulating method for converting an information signal into a multi-bit codeword sequence. In each codeword, the number of successive bits of a first logic value ("1") is at least

equal to P and groups of at least P bits of the first logic value are separated by at least Q successive bits of a second logic value ("0"), wherein P is an integer greater than or equal to 1 and Q is an integer greater than P. The number of bits of the first logic value is codeword-dependent.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a digital modulating method and a digital modulating apparatus with smaller crosstalk disturbance due to a pilot signal which is advantageous to high density recording.

A digital modulating method according to the present invention is defined by claim 1. The sub-claims 2 to 8 are directed to embodiments of the method.

In the digital modulating method according to the present invention, since the number of identical bits which are continuous in a 15-bit codeword sequence is not less than 2 and not more than 8, n=15, m=8, d=2 and k=8 in the expressions (1) and (2). Accordingly, from the expression (1), the minimum length between transitions Tmin is 1.07Tb and the maximal length between transitions Tmax is 4.27Tb. Also, from the expression (3), the density ratio DR is 1.07. As described above, the density ratio DR is larger than 1.

Also, since one of a plurality of 15-bit codewords assigned to each 8-bit data word is selected so that DSV at a last bit of each 15-bit codeword periodically varies, the periodical variation of DSV can be used as a pilot signal. Such a pilot signal does not give crosstalk disturbance to a reproduced signal in reproducing.

A digital modulating apparatus according to the present invention is defined by claim 9. The sub-claims 10 to 13 are directed to embodiments of the apparatus.

In the digital modulating apparatus according to the present invention, a 8-bit data word sequence is converted into a 15-bit codeword sequence so that a density ratio DR is larger than 1 and DSV at a last bit of each 15-bit codeword periodically changes. Accordingly, high density recording is enabled and also, the crosstalk disturbance due to a pilot signal can be avoided.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram illustrating a table of codewords sorted on the basis of initial two bits and CDS.

Fig. 2 is a diagram illustrating an example of assigning sorted codewords to 8-bit data words of 0 through 255.

Fig. 3 is a diagram illustrating an example of assigning four codewords to each 8-bit data word.

Fig. 4 is a diagram illustrating an example of assigning four codewords to each 8-bit data word.

Fig. 5 is a diagram illustrating an example of assigning four codewords to each 8-bit data word.

Fig. 6 is a diagram illustrating an example of assigning four codewords to each 8-bit data word.

Fig. 7 is a diagram illustrating an example of assigning four codewords to each 8-bit data word.

Fig. 8 is a diagram illustrating an example of assigning four codewords to each 8-bit data word.

Fig. 9 is a diagram illustrating an example of assigning four codewords to each 8-bit data word.

Fig. 10 is a diagram illustrating an example of assigning four codewords to each 8-bit data word.

Fig. 11 is a diagram illustrating a modulation example using the digital modulating method according to one embodiment of the present invention.

Fig. 12 is a diagram illustrating selection of codewords on the basis of control conditions.

Fig. 13 is a block diagram of a modulating circuit using the digital modulating method according to one embodiment of the present invention.

Fig. 14 is a diagram illustrating one example of tracking control with pilot signals of four frequencies.

Fig. 15 is a diagram illustrating relation among a data word, a codeword and a recording pattern.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figs. 1 through 12, a digital modulating method according to one embodiment of the present invention will be described.

In the digital modulating method of this embodiment, a 15-bit codeword corresponding to each 8-bit data word is determined according to the following procedures so that DSV at a final bit of each codeword periodically changes and also predetermined conditions are satisfied.

First, codes which satisfy the following conditions (1) through (4) are selected as candidates of codewords in 2^{15} of 15-bit codewords (hereinafter, simply referred to as a codeword).

(1) The number of continuous identical bits at a beginning portion of a codeword is 7 or smaller.
(2) The number of continuous identical bits at an ending portion of a codeword is 7 or smaller.
(3) The number of continuous identical bits is not less than 2 and not more than 8 from a second bit to a fourteenth bit in a codeword.
(4) An absolute value of CDS of a codeword is not more than 3.

With the conditions (1) through (3), the number of continuous identical bits can be not less than 2 and not more than 8 in a codeword sequence. Since the number of continuous same bits is 2 or larger in a codeword sequence, d=2 in expression (1). Accordingly, the minimum length between transitions Tmin is 1.07Tb. Also, since the number of continuous identical bits is 8 or smaller in a codeword sequence, k=8 in expression (2). Accordingly, the maximal length between transitions Tmax is 4.27Tb. Also, from expression (3), the density

ratio DR is 1.07. Although a shorter maximal length between transitions Tmax is more preferable, a maximum value of the number of identical bits which are continuous in a codeword sequence is set to 8 to facilitate production of 256 kinds of codewords corresponding to 256 of 8-bit data words.

Next, the candidates of codewords are respectively sorted into groups of codewords starting with "00", "01", "10" and "11", and each group of codewords is further sorted into codewords of which CDS are equal to +3, +1, - 1, -3, respectively. The numbers of codewords thus sorted are shown in Fig. 1.

For example, in the codewords beginning with "00", the number of codewords having CDS of +3, +1, -1, -3 are 54, 95, 120, 115, respectively.

Furthermore, for codewords respectively starting with "00", "01", "10", "11", first code pairs (+3, -1) are produced including codewords with CDS of +3 and codewords with CDS of -1 and second code pairs (+1, -3) are produced including codewords with CDS of +1 and codewords of CDS of -3.

One of the plurality of first code pairs (+3, -1) and one of the second code pairs (+1, -3) are assigned to each of 8-bit data words of 0 through 255. As described above, four codewords are assigned to each of the 8-bit data words. The number of code pairs sorted on the basis of initial two bits and the number of codeword pairs assigned to 8-bit data words are shown in Fig. 2.

For example, the number of first code pairs (+3, -1) including codewords beginning with "00" is 54, and 53 of the first code pairs (+3, -1) are assigned to 8-bit data words of 0 through 52. An example of assigning four codewords to each of 8-bit data words is shown in Figs. 3 through 10.

Now, combining conditions among codewords will be described. If codewords are selected according to the combining conditions (A) through (D) shown below, the number of continuing identical bits at combining portions among codewords can be not less than 2 and not more than 8.

(A) When last 2 bits of a preceding codeword are "00", a codeword starting with "11" or "01" is selected.
(B) When last 2 bits of a preceding codeword are "01", a codeword beginning with "11" or "10" is selected.
(C) When last 2 bits of a preceding codeword are "10", a codeword beginning with "00" or "01" is selected.
(D) When last 2 bits of a preceding codeword are "11", a codeword beginning with "00" or "10" is selected.

4 states

As seen from Fig. 2, regardless of the previous codeword, a code pair which satisfies the above-identified combining conditions (A) through (D) can be prepared for each 8-bit data word.

equivalent to a 4-state machine with 2 code words for each into word

For example, let us consider selection of codewords for 8-bit data words of 0 through 52. When last two bits of the previous codeword are "00" or "01", a second code pair (+1, -3) including codewords beginning with "11" can be selected. This satisfies the combining conditions (A) and (B). When final two bits of the previous codeword are "10" or "11", a first code pair (+3, -1) including codewords beginning with "00" can be selected. This satisfies the combining conditions (C) and (D).

According to the following control conditions (a), (b), a control value CD of DSV at the last bit of each codeword and a real value RD of DSV at the last bit of each codeword are determined. A control value of DSV at the last bit of each codeword is referred to as a control value of DSV and a real value of DSV at the last bit of each codeword is referred to as a real value of DSV, hereinafter. A control value CD of DSV means a target value of DSV which periodically changes.

(a) A difference between the current control value CD_n of DSV and the next control value CD_{n+1} of DSV is set to either one of -1, 0, +1.

If $CD_n - CD_{n+1}$ is set to -1, a control value CD of DSV changes in a positive direction, and if it is set to +1, a control value CD of DSV changes in the negative direction, and if it is set to 0, a control value CD of DSV maintains a constant value. From the control condition (a), the following expression holds.

$$-1 \leqq CD_n - CD_{n+1} \leqq 1 \quad (4)$$

Control values CD of DSV are set as shown in Fig. 11, for example.

(b) A difference between a present real value RD_n of DSV and a present control value CD_n of DSV is set to a value not less than -1 and not more than +2. Accordingly, the expression below holds.

$$-1 \leqq RD_n - CD_n \leqq 2 \quad (5)$$

On the basis of the control conditions (a) and (b), as shown in Fig. 12, one of codewords included in the first code pair (+3, -1) or one of codewords included in the second code pair (+1, -3) is selected as the next real value RD_{n+1} of DSV in a one-to-one manner. This will be described below.

$$A = CD_n - CD_{n+1} \quad (6)$$

$$B = RD_n - CD_n \quad (7)$$

Then, the expression below holds.

$$A + B = RD_n - CD_{n+1} \quad (8)$$

The expression below holds from expression (5).

$$-1 \leqq RD_{n+1} - CD_{n+1} \leqq 2 \quad (9)$$

The expression below holds from expressions (8)

and (9).

$$-1-(A+B) \leqq RD_{n+1}-RD_n \leqq 2-(A+B) \quad (10)$$

$RD_{n+1} - RD_n$ is equal to CDS of the next codeword.

On the other hand, from expressions (4) and (5), the following expression holds.

$$-2 \leqq A+B\ (=RD_n-CD_{n+1}) \leqq 3 \quad (11)$$

Accordingly, A + B takes a value of 3 through -2.

When A + B = 3, from expression (10), -4 ≦ CDS ≦ -1 holds. Accordingly, a codeword with CDS equal to -1 or -3 is selected.

If A + B = 2, from expression (10), -3 ≦ CDS ≦ 0 holds. Accordingly, a codeword with CDS equal to -1 or -3 is selected.

If A + B = 1, from expression (10), -2 ≦ CDS ≦ 1 holds. Accordingly, a codeword having CDS equal to +1 or -1 is selected.

If A + B = 0, from expression (10), -1 ≦ CDS ≦ 2 holds. Accordingly, a codeword having CDS of +1 or -1 is selected.

If A + B = -1, from expression (10), 0 ≦ CDS ≦ 3 holds. Accordingly, a codeword with CDS of +1 or +3 is selected.

If A + B = -2, from expression (10), 1 ≦ CDS ≦ 4 holds. Accordingly, a codeword with CDS equal to +3 or +1 is selected.

In summary, if A + B is 3 or 2, a codeword with CDS of -1 or -3 is selected. If A + B is equal to 1 or 0, a codeword having CDS equal to +1 or -1 is selected. If A + B is -1 or -2, a codeword with CDS equal to +3 or +1 is selected.

As described above, a real value RD of DSV varies inside a zone which changes periodically as shown by a broken line in Fig. 11. Accordingly, tracking control can be applied by using the DSV as a pilot signal.

Fig. 13 is a block diagram of a 8-15 modulating circuit using the digital modulating method of this embodiment.

A DSV control value output unit 1 controls amplitude and frequency of a pilot signal by controlling DSV. DSV control value output unit 1 provides a vector signal ($CD_n - CD_{n+1}$) for DSV control as an output. The vector signal indicates either one of "-1", "0", "+1" by the DSV control condition (a). When the vector signal indicates "-1", a DSV control value CD changes in a positive direction, when it indicates "+1", it changes in a negative direction, and if it indicates "0", it maintains a constant value (refer to Fig. 11).

An adder 2 obtains a sum of values applied to three input terminals a, b, c and provides the sum as an output from an output terminal. A difference between a current real value RD_n of DSV and a current control value CD_n of DSV, (RDn-CDn), is applied to input terminal a and a vector signal ($CD_n - CD_{n+1}$) for DSV control is applied to input terminal b. A value ($RD_{n-1} - RD_n$) of CDS of a codeword selected by a 8-15 converting unit 6 which will be described later is applied to input terminal c. Accordingly, a sum thereof ($RD_{n+1} - CD_{n+1}$) is provided as an output from the output terminal of adder 2. The sum attains "-1" through "+2" (refer to expression (9)). An output of adder 2 is latched in a latch circuit 3. An output of latch circuit 3 indicates a difference ($RD_n - CD_n$) between a current real value RD_n of DSV and a current control value CD_n of DSV.

A sum of values provided to two input terminals a, b is found by adder 4, which is outputted from an output terminal. A vector signal ($CD_n - CD_{n+1}$) for DSV control is applied to input terminal a and an output ($RD_n - CD_n$) of latch circuit 3 is applied to input terminal b. Accordingly, a sum ($RD_n - CD_{n+1}$) of those values is outputted from the output terminal of adder 4. The sum is "-2" through "+3" from control conditions of DSV (refer to expression (11)).

A comparator 5 provides a control signal a to 8-15 converting unit 6 when an output of adder 4 is "+3" or "+2", provides a control signal b to 8-15 converting unit 6 when an output thereof is "+1" or "0", and provides a control signal c to 8-15 converting unit 6 when an output thereof is "-1" or "-2". Latch circuit 7 temporarily stores last two bits of a codeword.

8-15 converting unit 6 receives a 8-bit data word and provides a codeword as an output. That is, 8-15 converting unit 6 selects one of codewords on the basis of an inputted 8-bit data word, a control signal from comparator 5 and last two bits of the previous codeword stored in latch circuit 7 and provides the same as an output. 8-15 converting unit 6 selects a codeword with CDS of -1 or -3 when a control signal is "a", selects a codeword with CDS of +1 or -1 when a control signal is "b", and selects a codeword with CDS of +3 or +1 when a control signal is "c". Simultaneously, 8-15 converting unit 6 applies the last two bits of a codeword to latch circuit 7 and also provides a value ($RD_{n+1} - RD_n$) of CDS of that codeword to adder 2.

A codeword (parallel data) outputted from 8-15 converting unit 6 is converted into 15-bit serial data (15-bit serial modulation signal) by a P-S (Parallel - Serial) converting unit 8.

For example, in Fig. 11, if $RD_n - CD_n = 0$, $CD_n - CD_{n+1} = -1$, then $A + B = RD_n - CD_{n+1} = -1$. Accordingly, a control signal is "c". Therefore, a codeword with CDS equal to +3 or +1 is selected. When a first code pair (+3, -1) is selected, a codeword with CDS of +3 is selected, and when a second code pair (+1, -3) is selected, a codeword of CDS of +1 is selected. As in the example shown in Fig. 11, when a first code pair (+3, -1) is selected on the basis of an inputted 8-bit data word and the last two bits of the previous codeword, a codeword with CDS equal to +3 is selected. Thus, $RD_{n+1} - RD_n = +3$. As a result, $RD_{n+1} - CD_{n+1} = +2$.

As described above, a pilot signal necessary for the ATF method or the DTF method is obtained.

Next, an example of tracking control using the digital modulating method of this embodiment will be described.

For example, let a recording rate be 30Mbps (bit per second). In this digital modulating method, DSV control is performed in 8-bit units, so that a reference frequency f_{word} is 30MHz / 8 = 3.75MHz. The reference frequency f_{word} is frequency-divided as described below.

$f_1 = f_{word} / 28 = 133.9KHz$
$f_2 = f_{word} / 32 = 117.2KHz$
$f_3 = f_{word} / 46 = 81.5KHz$
$f_4 = f_{word} / 38 = 98.7KHz$

Codewords are determined so that values of DSV at the last bits of codewords change at these frequencies f_1 - f_4. The DSVs which vary at frequencies f_1 - f_4 are used as pilot signals of four frequencies. That is, one period includes 28 codewords in a pilot signal of frequency f_1, one period includes 32 codewords in a pilot signal of frequency f_2, one period includes 46 codewords in a pilot signal of frequency f_3, and one period includes 38 codewords in a pilot signal of frequency f_4.

Control values CD of DSV are sequentially provided as outputs from DSV control value output unit 1 of Fig. 13 so that frequencies of pilot signals differ for each track. 15-bit serial data outputted from P-S converting unit 8 is recorded in tracks T1 - T4 shown in Fig. 14. Pilot signals with frequencies which are different for each track are thus recorded.

When reproducing, a pilot signal recorded in each of respective tracks T1 - T4 is reproduced, and a frequency of that pilot signal and a reference signal with the same frequency are multiplied. If the frequency of the pilot signal differs from the frequency of the reference signal, beat occurs corresponding to the difference of frequency. The frequency of the difference is extracted by a band-pass filter or the like and tracking information is obtained.

The digital modulating method of this embodiment can also be applied to tracking control methods with pilot signals of one frequency, two frequencies or other numbers of frequencies, as well as pilot signals of four frequencies.

As described above, according to the present invention, the number of identical bits which are continuous in a 15-bit codeword sequence is not less than 2 and not more than 8, and DSV at a last bit of each 15-bit codeword periodically varies. Accordingly, the density ratio increases and the periodical variation of DSV can be used as a pilot signal. As a result, high density recording is enabled and tracking control is also enabled in which a reproduced signal does not suffer from cross-talk disturbance due to a pilot signal.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being defined by the terms of the appended claims.

Claims

1. A digital modulating method for converting an 8-bit data word sequence into a 15-bit codeword sequence, comprising the steps of:

   assigning a plurality of 15-bit codewords to each 8-bit data word so that the number of continuous identical bits is not less than 2 and not more than 8 in the 15-bit codeword sequence; and
   selecting one of the plurality of 15-bit codewords assigned to each 8-bit data word so that Digital Sum Variation at a last bit of each 15-bit codeword periodically changes, wherein:
   said assigning step comprises producing a plurality of first code pairs each including a 15-bit codeword with Code-word Digital Sum of +3 and a 15-bit codeword with Code-word Digital Sum of -1 and a plurality of second code pairs each including a 15-bit codeword with Code-word Digital Sum of +1 and a 15-bit codeword with Code-word Digital Sum of -3, assigning one of said plurality of first code pairs and one of said plurality of second code pairs to each 8-bit data word, and selecting one of the first and second code pairs assigned to each 8-bit data word so that the number of continuous identical bits is not less than 2 and not more than 8 in the 15-bit codeword sequence; and
   said selecting step comprises selecting one of two 15-bit codewords included in the selected code pair so that Digital Sum Variation at a last bit of each 15-bit codeword periodically varies.

2. The digital modulating method according to claim 1, wherein said producing step comprises:

   selecting 15-bit codewords as candidates out of 15-bit codewords, which satisfy conditions: (1) the number of continuous identical bits is not more than 7 at a beginning portion of a 15-bit codeword,(2) the number of continuous identical bits is not more than 7 at an ending portion of a 15-bit codeword, (3) the number of continuous identical bits from a second bit to a fourteenth bit of a 15-bit codeword is not less than 2 and not more than 8, and (4) an absolute value of Code-word Digital Sum of a 15-bit codeword is not more than 3;
   sorting the selected 15-bit codewords as candidates into a group including 15-bit codewords beginning with 00, a group including 15-bit codewords beginning with 01, a group including

15-bit codewords beginning with 10 and a group including 15-bit codewords beginning with 11;

sorting 15-bit codewords included in each group into 15-bit codewords with Code-word Digital Sum of +3, 15-bit codewords with Code-word Digital Sum of +1, 15-bit codewords with Code-word Digital Sum of -1 and 15-bit codewords with Code-word Digital Sum of -3; and

producing first code pairs each including a 15-bit codeword with Code-word Digital Sum of +3 and a 15-bit codeword with Code-word Digital Sum of -1 and producing second code pairs each including a 15-bit codeword with Code-word Digital Sum of +1 and a 15-bit codeword with Code-word Digital Sum of -3 in each of the group of 15-bit codewords beginning with 00, the group of 15-bit codewords beginning with 01, the group of 15-bit codewords beginning with 10 and the group of 15-bit codewords beginning with 11.

3. The digital modulating method according to claim 2, wherein said step of selecting one of said first and second code pairs comprises: (A) selecting a 15-bit codeword beginning with 11 or 01 when last two bits of a preceding 15-bit codeword are 00, (B) selecting a 15-bit codeword beginning with 11 or 10 when last two bits of a preceding 15-bit codeword are 01, (C) selecting a 15-bit codeword beginning with 00 or 01 when last two bits of a preceding 15-bit codeword are 10, and (D) selecting a 15-bit codeword beginning with 00 or 10 when last two bits of a preceding 15-bit codeword are 11.

4. The digital modulating method according to claim 1, wherein said step of selecting one of said two 15-bit codewords comprises :

determining a control value of Digital Sum Variation at a last bit of each 15-bit codeword and a real value of Digital Sum Variation at a last bit of each 15-bit codeword and selecting one of two 15-bit codewords included in the selected code pair on the basis of said determined Digital Sum Variation control value and the Digital Sum Variation real value;

wherein said Digital Sum Variation control value represents a target value of Digital Sum Variation which periodically varies.

5. The digital modulating method according to claim 4, wherein said determining step comprises setting a difference between a control value of Digital Sum Variation at a last bit of a current 15-bit codeword and a control value of Digital Sum Variation at a last bit of a next 15-bit codeword to one of predetermined values and setting a difference between a real value of Digital Sum Variation at a last bit of a current 15-bit codeword and a control value at a last bit of a current 15-bit codeword within a predetermined range.

6. The digital modulating method according to claim 5, wherein said step of selecting one of two 15-bit codewords comprises selecting one of said two 15-bit codewords so that a difference between a real value of Digital Sum Variation at a last bit of a current 15-bit codeword and a control value of Digital Sum Variation at a last bit of a next 15-bit codeword is within a predetermined range.

7. The digital modulating method according to claim 5, wherein said predetermined value includes -1, 0 and +1, and said predetermined range is not less than -1 and not more than 2.

8. The digital modulating method according to claim 6, wherein said predetermined range is not less than -2 and not more than +3.

9. A digital modulating apparatus for converting an 8-bit data word sequence into a 15-bit codeword sequence, comprising:

control means (1) for generating a control signal for periodically changing Digital Sum Variation at a last bit of each 15-bit codeword; and

converting means (2 - 7) for sequentially converting each 8-bit data word into a 15-bit codeword so that the number of continuous identical bits is not less than 2 and not more than 8 in a 15-bit codeword sequence in response to a control signal from said control means (1);

wherein said converting means (2 - 7) produces a plurality of first code pairs each including a 15-bit codeword with Code-word Digital Sum of +3 and a 15-bit codeword with Code-word Digital Sum of -1 and a plurality of second code pairs each including a 15-bit codeword with Code-word Digital Sum of +1 and a 15-bit codeword with Code-word Digital Sum of -3, assigns one of said plurality of first code pairs and one of said plurality of second code pairs to each 8-bit data word, selects one of the first and second code pairs assigned to each 8-bit data word so that the number of continuous identical bits is not less than 2 and not more than 8 in a 15-bit codeword sequence, and selects one of two 15-bit codewords included in the selected code pair so that Digital Sum Variation at a last bit of each 15-bit codeword periodically varies.

10. The digital modulating apparatus according to claim 9, wherein:

said control signal represents a difference be-

tween a control value of Digital Sum Variation at a last bit of a current 15-bit codeword and a control value of Digital Sum Variation at a last bit of a next 15-bit codeword, and said control value of Digital Sum Variation represents a target value of Digital Sum Variation which periodically changes; and
said converting means (2 - 7) converts each 8-bit data word into a 15-bit codeword on the basis of a difference between a control value of Digital Sum Variation at a last bit of a current 15-bit codeword and a control value of Digital Sum Variation at a last bit of 15-bit codeword and a real value of Digital Sum Variation at a last bit of a current 15-bit codeword.

11. The digital modulating apparatus according to claim 10, wherein said converting means comprises:

first adding means (2);
first holding means (3) for temporarily holding an output of said first adding means (2);
second adding means (4);
signal generating means (5) for generating a selection signal in response to an output of said second adding means (4);
8-15 converting means (6);
output means (6) for outputting a difference between a real value of Digital Sum Variation at a last bit of a next 15-bit codeword and a real value of Digital Sum Variation at a last bit of a current 15-bit codeword; and
second holing means (7) for temporarily holding last two bits of a 15-bit codeword, wherein:
said first adding means (2) adds an output of said control means (1), an output of said first holding means (3) and an output of said output means (6);
said second adding means (4) adds an output of said control means (1) and an output of said first holding means (3); and
said 8-15 converting means (6) selects and outputs one of said 15-bit codewords on the basis of an inputted 8-bit data word, said selection signal and an output of said second holding means (7).

12. The digital modulating apparatus according to claim 11, wherein:

said signal generating means (5) generates a first control signal when an output of said second adding means (4) is a first value, generates a second control signal when an output of said second adding means (4) is a second value, and generates a third control signal when an output of said second adding means (4) is a third value; and
said 8-15 converting means (6) selects a 15-bit codeword with Code-word Digital Sum of -1 or -3 in response to said first selection signal, selects a 15-bit codeword with Code-word Digital Sum of +1 or -1 in response to said second control signal, and selects a 15-bit codeword with Code-word Digital Sum of +3 or +1 in response to said third control signal.

13. The digital modulating apparatus according to claim 11, further comprising parallel/serial converting means (8) for converting a 15-bit codeword outputted from said 8-15 converting means (6) into a 15-bit serial modulated signal.

Patentansprüche

1. Verfahren zur digitalen Modulation zum Umsetzen einer 8-Bit-Datenwortfolge in eine 15-Bit-Codewortfolge, mit den folgenden Schritten:

- Zuordnen mehrerer 15-Bit-Codewörter zu jedem 8-Bit-Datenwort in solcher Weise, daß die Anzahl aufeinanderfolgender identischer Bits in der 15-Bit-Codewortfolge nicht kleiner als 2 und nicht größer als 8 ist; und
- Auswählen eines der mehreren jedem 8-Bit-Datenwort zugeordneten 15-Bit-Codewörter in solcher Weise, daß sich der Wert der digitalen Summenänderung am letzten Bit jedes 15-Bit-Codeworts periodisch ändert, wobei:
- der Zuordnungsschritt folgendes umfaßt: Erzeugen mehrerer erster Codepaare, von denen jedes ein 15-Bit-Codewort mit einer Codewort-Digitalsumme +3 und ein 15-Bit-Codewort mit einer Codewort-Digitalsumme -1 enthält, und mehrerer zweiter Codepaare, von denen jedes ein 15-Bit-Codewort mit einer Codewort-Digitalsumme +1 und ein 15-Bit-Codewort mit einer Codewort-Digitalsumme -3 enthält, Zuordnen eines der mehreren ersten Codepaare und eines der mehreren zweiten Codepaare zu jedem 8-Bit-Datenwort, und Auswählen des ersten oder zweiten Codepaars, wie sie jedem 8-Bit-Datenwort zugeordnet sind, in solcher Weise, daß die Anzahl aufeinanderfolgender identischer Bits innerhalb der 15-Bit-Codewortfolge nicht kleiner als 2 und nicht größer als 8 ist; und
- der Auswahlschritt das Auswählen eines von zwei 15-Bit-Codewörtern umfaßt, die im ausgewählten Codepaar enthalten sind, in solcher Weise, daß sich der Wert der digitalen Summenänderung am letzten Bit jedes 15-Bit-Codeworts periodisch ändert.

2. Verfahren zur digitalen Modulation nach Anspruch

1, bei dem der Erzeugungsschritt folgendes umfaßt:

- Auswählen von 15-Bit-Codewörtern als Kandidaten aus 15-Bit-Codewörtern, die die folgenden Bedingungen erfüllen: (1) die Anzahl aufeinanderfolgender identischer Bits ist im Anfangsabschnitt eines 15-Bit-Codeworts nicht größer als 7, (2) die Anzahl aufeinanderfolgender identischer Bits ist im Endabschnitt eines 15-Bit-Codeworts nicht größer als 7, (3) die Anzahl aufeinanderfolgender identischer Bits ist ab dem zweiten Bit bis zum vierzehnten Bit eines 15-Bit-Codeworts nicht kleiner als 2 und nicht größer als 8 und (4) der Absolutwert der Codewort-Digitalsumme eines 15-Bit-Codeworts ist nicht größer als 3;
- Sortieren der ausgewählten 15-Bit-Codewörter als Kandidaten in eine Gruppe von mit 00 beginnenden 15-Bit-Codewörtern; eine Gruppe von mit 01 beginnenden 15-Bit-Codewörtern, eine Gruppe von mit 10 beginnenden 15-Bit-Codewörtern und eine Gruppe von mit 11 beginnenden Codewörtern;
- Sortieren der 15-Bit-Codewörter in jeder Gruppe in 15-Bit-Codewörter mit der Codewort-Digitalsumme +3, 15-Bit-Codewörter mit der Codewort-Digitalsumme +1, 15-Bit-Codewörter mit der Codewort-Digitalsumme -1 und 15-Bit-Codewörter mit der Codewort-Digitalsumme -3; und
- Erzeugen erster Codepaare, von denen jedes ein 15-Bit-Codewort mit der Codewort-Digitalsumme +3 und ein 15-Bit-Codewort mit der Codewort-Digitalsumme -1 enthält, und Erzeugen zweiter Codepaare, von denen jedes ein 15-Bit-Codewort mit der Codewort-Digitalsumme +1 und ein 15-Bit-Codewort mit der Codewort-Digitalsumme -3 enthält, und zwar in jeder der folgenden Gruppen: der Gruppe von mit 00 beginnenden 15-Bit-Codewörtern, der Gruppe von mit 01 beginnenden 15-Bit-Codewörtern, der Gruppe von mit 10 beginnenden 15-Bit-Codewörtern und der Gruppe von mit 11 beginnenden 15-Bit-Codewörtern.

3. Verfahren zur digitalen Modulation nach Anspruch 2, bei dem der Schritt des Auswählens des ersten oder zweiten Codepaars folgendes umfaßt: (A) Auswählen eines mit 11 oder 01 beginnenden 15-Bit-Codeworts, wenn die letzten zwei Bits des vorangehenden 15-Bit-Codeworts 00 sind, (B) Auswählen eines mit 11 oder 10 beginnenden 15-Bit-Codeworts, wenn die letzten zwei Bits des vorangehenden 15-Bit-Codeworts 01 sind, (C) Auswählen eines mit 00 oder 01 beginnenden 15-Bit-Codeworts, wenn die letzten zwei Bits des vorangehenden 15-Bit-Codeworts 10 sind, und (D) Auswählen eines mit 00 oder 10 beginnenden 15-Bit-Codeworts, wenn die letzten zwei Bits des vorangehenden 15-Bit-Codeworts 11 sind,

4. Verfahren zur digitalen Modulation nach Anspruch 1, bei dem der Schritt des Auswählens eines der zwei 15-Bit-Codewörter folgendes umfaßt:

- Bestimmen eines Steuerwerts zum Wert der digitalen Summenänderung am letzten Bit jedes 15-Bit-Codeworts sowie eines reellen Werts des Werts der digitalen Summenänderung am letzten Bit jedes 15-Bit-Codeworts, und Auswählen eines der zwei 15-Bit-Codewörter im ausgewählten Codepaar auf Grundlage des bestimmten Steuerwerts für den Wert der digitalen Summenänderung und des reellen Werts des Werts der digitalen Summenänderung;
- wobei der Steuerwert für den Wert der digitalen Summenänderung einen Sollwert für die digitale Summenänderung repräsentiert, der sich periodisch ändert.

5. Verfahren zur digitalen Modulation nach Anspruch 4, bei dem der Bestimmungsschritt folgendes umfaßt: Einstellen der Differenz zwischen dem Steuerwert des Werts der digitalen Summenänderung am letzten Bit eines aktuellen 15-Bit-Codeworts und des Steuerwerts des Werts der digitalen Summenänderung am letzten Bit des nächsten 15-Bit-Codeworts auf einen von mehreren vorgegebenen Werten, und Einstellen der Differenz zwischen dem reellen Wert des Werts der digitalen Summenänderung am letzten Bit des aktuellen 15-Bit-Codeworts und dem Steuerwert am letzten Bit des aktuellen 15-Bit-Codeworts in einem vorbestimmten Bereich.

6. Verfahren zur digitalen Modulation nach Anspruch 5, bei dem der Schritt des Auswählens eines der zwei 15-Bit-Codewörter folgendes umfaßt: Auswählen eines der zwei 15-Bit-Codewörter in solcher Weise, daß die Differenz zwischen dem reellen Wert des Werts der digitalen Summenänderung am letzten Bit des aktuellen 15-Bit-Codeworts und dem Steuerwert des Werts der digitalen Summenänderung am letzten Bit des nächsten 15-Bit-Codeworts in einem vorbestimmten Bereich liegt.

7. Verfahren zur digitalen Modulation nach Anspruch 5, bei dem der vorbestimmte Wert -1, 0 und +1 umfaßt und der vorbestimmte Bereich nicht kleiner als -1 und nicht größer als 2 ist.

8. Verfahren zur digitalen Modulation nach Anspruch 6, bei dem der vorgegebene Bereich nicht kleiner als -2 und nicht größer als +3 ist.

9. Vorrichtung zur digitalen Modulation zum Umset-

zen einer 8-Bit-Datenwortfolge in eine 15-Bit-Codewortfolge, mit:

- einer Steuereinrichtung (1) zum Erzeugen eines Steuersignals zum periodischen Ändern des Werts der digitalen Summenänderung am letzten Bit jedes 15-Bit-Codeworts; und
- einer Umsetzeinrichtung (2 - 7) zum sequentiellen Umsetzen, auf ein Steuersignal von der Steuereinrichtung (1) hin, jedes 8-Bit-Datenworts in solcher Weise in ein 15-Bit-Codewort, daß die Anzahl aufeinanderfolgender identischer Bits in einer 15-Bit-Codewortfolge nicht kleiner als 2 und nicht größer als 8 ist;
- wobei die Umsetzeinrichtung (2 - 7) mehrere erste Codepaare, von denen jedes ein 15-Bit-Codewort mit einer Codewort-Digitalsumme +3 und ein 15-Bit-Codewort mit einer Codewort-Digitalsumme -1 enthält, und mehrere zweite Codepaare, von denen jedes ein 15-Bit-Codewort mit einer Codewort-Digitalsumme +1 und ein 15-Bit-Codewort mit einer Codewort-Digitalsumme -3 enthält, erzeugt, sie eines der mehreren ersten Codepaare und eines der mehreren zweiten Codepaare jedem 8-Bit-Datenwort zuordnet, sie vom ersten und zweiten Codepaar, wie sie jedem 8-Bit-Datenwort zugeordnet sind, eines so auswählt, daß die Anzahl aufeinanderfolgender identischer Bits in einer 15-Bit-Codewortfolge nicht kleiner als 2 und nicht größer als 8 ist, und sie eines der im ausgewählten Codepaar enthaltenen zwei 15-Bit-Codewörter so auswählt, daß sich der Wert der digitalen Summenänderung am letzten Bit jedes 15-Bit-Codeworts periodisch ändert.

10. Vorrichtung zur digitalen Modulation nach Anspruch 9, bei der:

- das Steuersignal die Differenz zwischen dem Steuerwert des Werts der digitalen Summenänderung am letzten Bit des aktuellen 15-Bit-Codeworts und dem Steuerwort des Werts der digitalen Summenänderung am letzten Bit des nächsten 15-Bit-Codeworts repräsentiert, und der Steuerwert des Werts der digitalen Summenänderung den Sollwert der digitalen Summenänderung repräsentiert, der sich periodisch ändert; und
- die Umsetzeinrichtung (2 - 7) jedes 8-Bit-Datenworts auf Grundlage der Differenz zwischen dem Steuerwert des Werts der digitalen Summenänderung am letzten Bit des aktuellen 15-Bit-Codeworts und dem Steuerwert des Werts der digitalen Summenänderung am letzten Bit des 15-Bit-Codeworts und dem reellen Wert des Werts der digitalen Summenänderung am letzten Bit des aktuellen 15-Bit-Codeworts in ein 15-Bit-Codewort umsetzt.

11. Vorrichtung zur digitalen Modulation nach Anspruch 10, bei dem die Umsetzeinrichtung folgendes aufweist:

- eine erste Addiereinrichtung (2);
- eine erste Speichereinrichtung (3) zum Zwischenspeichern des Ausgangssignals der ersten Addiereinrichtung (2);
- eine zweite Addiereinrichtung (4);
- eine Signalerzeugungseinrichtung (5) zum Erzeugen eines Auswahlsignals auf das Ausgangssignal der zweiten Addiereinrichtung (4) hin;
- eine 8-15-Umsetzeinrichtung (6);
- eine Ausgabeeinrichtung (6) zum Ausgeben der Differenz zwischen dem reellen Wert des Werts der digitalen Summenänderung am letzten Bit des nächsten 15-Bit-Codeworts und dem reellen Wert des Werts der digitalen Summenänderung am letzten Bit des aktuellen 15-Bit-Codeworts; und
- eine zweite Speichereinrichtung (7) zum Zwischenspeichern der letzten zwei Bits eines 15-Bit-Codeworts; wobei:
- die erste Addiereinrichtung (2) das Ausgangssignal der Steuereinrichtung (1), das Ausgangssignal der ersten Speichereinrichtung (3) und das Ausgangssignal der Ausgabeeinrichtung (6) addiert;
- die zweite Addiereinrichtung (4) das Ausgangssignal der Steuereinrichtung (1) und das Ausgangssignal der ersten Speichereinrichtung (3) addiert; und
- die 8-15-Umsetzeinrichtung (6) eines der 15-Bit-Codewörter auf Grundlage des eingegebenen 8-Bit-Datenworts, des Auswahlsignals und des Ausgangssignal der zweiten Speichereinrichtung (7) auswählt und ausgibt.

12. Vorrichtung zur digitalen Modulation nach Anspruch 11, bei der:

- die signalerzeugungseinrichtung (5) ein erstes Steuersignal erzeugt, wenn das Ausgangssignal der zweiten Addiereinrichtung (4) einen ersten Wert hat, sie ein zweites Steuersignal erzeugt, wenn das Ausgangssignal der zweiten Addiereinrichtung (4) einen zweiten Wert hat, und sie ein drittes Steuersignal erzeugt, wenn das Ausgangssignal der zweiten Addiereinrichtung (4) einen dritten Wert hat; und
- die 8-15-Umsetzeinrichtung (6) auf das erste Auswahlsignal hin ein 15-Bit-Codewort mit einer Codewort-Digitalsumme von
- 1 oder -3 auswählt, sie auf das zweite Steuersignal ein 15-Bit-Codewort mit einer Codewort-

Digitalsumme von +1 oder -1 auswählt, und sie auf das dritte Steuersignal ein 15-Bit-Codewort mit einer Codewort-Digitalsumme von +3 oder +1 auswählt.

13. Vorrichtung zur digitalen Modulation nach Anspruch 11, ferner mit einer Parallel/seriell-Umsetzeinrichtung (8) zum Umsetzen eines von der 8-15-Umsetzeinrichtung (6) ausgegebenen 15-Bit-Codeworts in ein serielles, moduliertes 15-Bit-Signal.

Revendications

1. Procédé de modulation numérique destiné à convertir une séquence de mots de données de 8 bits en une séquence de mots de code de 15 bits, comportant les étapes consistant:

à affecter une multiplicité de mots de code de 15 bits à chaque mot de données de 8 bits de sorte que le nombre de bits identiques consécutifs ne soit pas inférieur à 2 et ne soit pas supérieur à 8 dans la séquence de mots de code de 15 bits; et
à sélectionner un mot de code de la multiplicité de mots de code de 15 bits affectés à chaque mot de données de 8 bits de sorte que la variation de somme numérique au niveau d'un dernier bit de chaque mot de code de 15 bits change périodiquement, dans lequel:
ladite étape d'affectation consiste à produire une multiplicité de premières paires de codes comprenant chacune un mot de code de 15 bits ayant une somme numérique de mot de code de +3 et un mot de code de 15 bits ayant une somme numérique de mot de code de -1, ainsi qu'une multiplicité de secondes paires de codes comprenant chacune un mot de code de 15 bits ayant une somme numérique de mot de code de +1 et un mot de code de 15 bits ayant une somme numérique de mot de code de -3, à affecter une des paires de ladite multiplicité de premières paires de codes et une des paires de ladite multiplicité de secondes paires de codes à chaque mot de données de 8 bits, et à sélectionner une des première et seconde paires de codes affectées à chaque mot de données de 8 bits de sorte que le nombre de bits identiques consécutifs ne soit pas inférieur à 2 et ne soit pas supérieur à 8 dans la séquence de mots de code de 15 bits; et
ladite étape de sélection consiste à sélectionner l'un de deux mots de code de 15 bits compris dans la paire de codes sélectionnés de sorte que la variation de somme numérique au niveau d'un dernier bit de chaque mot de code de 15 bits varie périodiquement.

2. Procédé de modulation numérique selon la revendication 1, dans lequel ladite étape de production consiste:

à sélectionner des mots de code de 15 bits en tant que candidats parmi des mots de code de 15 bits qui remplissent les conditions suivantes: (1) le nombre de bits identiques consécutifs n'est pas supérieur à 7 au niveau d'une partie initiale d'un mot de code de 15 bits, (2) le nombre de bits identiques consécutifs n'est pas supérieur à 7 au niveau d'une partie finale d'un mot de code de 15 bits, (3) le nombre de bits identiques consécutifs, allant d'un second bit jusqu'à un quatorzième bit, d'un mot de code de 15 bits n'est pas inférieur à 2 et n'est pas supérieur à 8, et (4) une valeur absolue d'une somme numérique de mot de code d'un mot de code de 15 bits n'est pas supérieure à 3;
à trier les mots de code de 15 bits sélectionnés en tant que candidats pour former un groupe comprenant des mots de code de 15 bits commençant par 00, un groupe comprenant des mots de code de 15 bits commençant par 01, un groupe comprenant des mots de code de 15 bits commençant par 10 et un groupe comprenant des mots de code de 15 bits commençant par 11;
à trier des mots de code de 15 bits compris dans chaque groupe pour obtenir des mots de code de 15 bits ayant une somme numérique de mot de code de +3, des mots de code de 15 bits ayant une somme numérique de mot de code de +1, des mots de code de 15 bits ayant une somme numérique de mot de code de -1 et des mots de code de 15 bits ayant une somme numérique de mot de code de -3, et
à produire des premières paires de codes comprenant chacune un mot de code de 15 bits ayant une somme numérique de mot de code de +3 et un mot de code de 15 bits ayant une somme numérique de mot de code de -1 et à produire des secondes paires de codes comprenant chacune un mot de code de 15 bits ayant une somme numérique de mot de code de +1 et un mot de code de 15 bits ayant une somme numérique de mot de code de -3 dans chacun des groupes suivants: le groupe de mots de code de 15 bits commençant par 00, le groupe de mots de code de 15 bits commençant par 01, le groupe de mots de code de 15 bits commençant par 10 et le groupe de mots de code de 15 bits commençant par 11.

3. Procédé de modulation numérique selon la revendication 2, dans lequel ladite étape de sélection

d'une desdites première et seconde paires de codes consiste: (A) à sélectionner un mot de code de 15 bits commençant par 11 ou 01 lorsque les deux derniers bits d'un mot de code de 15 bits précédent sont 00, (B) à sélectionner un mot de code de 15 bits commençant par 11 ou 10 lorsque les deux derniers bits d'un mot de code de 15 bits précédent sont 01, (C) à sélectionner un mot de code de 15 bits commençant par 00 ou 01 lorsque les deux derniers bits d'un mot de code de 15 bits précédent sont 10, et (D) à sélectionner un mot de code de 15 bits commençant par 00 ou 10 lorsque les deux derniers bits d'un mot de code de 15 bits précédent sont 11.

4. Procédé de modulation numérique selon la revendication 1, dans lequel ladite étape de sélection de l'un desdits deux mots de code de 15 bits consiste:

à déterminer une valeur de contrôle de variation de somme numérique au niveau d'un dernier bit de chaque mot de code de 15 bits et une valeur réelle de variation de somme numérique au niveau d'un dernier bit de chaque mot de code de 15 bits et à sélectionner l'un de deux mots de code de 15 bits compris dans la paire de codes sélectionnée sur la base de ladite valeur de contrôle de variation de somme numérique déterminée et de la valeur réelle de variation de somme numérique;
dans lequel ladite valeur de contrôle de variation de somme numérique représente une valeur cible de variation de somme numérique qui varie périodiquement.

5. Procédé de modulation numérique selon la revendication 4, dans lequel ladite étape de détermination consiste à sélectionner, pour une différence entre une valeur de contrôle de variation de somme numérique au niveau d'un dernier bit d'un mot de code de 15 bits courant et une valeur de contrôle de variation de somme numérique au niveau d'un dernier bit d'un mot de code de 15 bits suivant, une valeur parmi des valeurs prédéterminées et à sélectionner, pour une différence entre une valeur réelle de variation de somme numérique au niveau d'un dernier bit d'un mot de code de 15 bits courant et une valeur de contrôle au niveau d'un dernier bit d'un mot de code de 15 bits courant, une valeur se situant dans une gamme prédéterminée.

6. Procédé de modulation numérique selon la revendication 5, dans lequel ladite étape de sélection de l'un de deux mots de code de 15 bits consiste à sélectionner l'un desdits deux mots de code de 15 bits de sorte qu'une différence entre une valeur réelle de variation de somme numérique au niveau d'un dernier bit d'un mot de code de 15 bits courant et une valeur de contrôle de variation de somme numérique au niveau d'un dernier bit d'un mot de code de 15 bits suivant se situe dans une gamme prédéterminée.

7. Procédé de modulation numérique selon la revendication 5, dans lequel ladite valeur prédéterminée comprend -1, 0 et +1 et les limites de ladite gamme prédéterminée ne sont pas inférieures à -1 et ne sont pas supérieures à 2.

8. Procédé de modulation numérique selon la revendication 6, dans lequel les limites de ladite gamme prédéterminée ne sont pas inférieures à -2 et ne sont pas supérieures à +3.

9. Appareil de modulation numérique pour convertir une séquence de mots de données de 8 bits en une séquence de mots de code de 15 bits, comportant:

des moyens de commande (1) pour générer un signal de commande pour modifier périodiquement une variation de somme numérique au niveau d'un dernier bit de chaque mot de code de 15 bits; et
des moyens de conversion (2 - 7) pour convertir séquentiellement chaque mot de données de 8 bits en un mot de code de 15 bits de sorte que le nombre de bits identiques consécutifs ne soit pas inférieur à 2 et ne soit pas supérieur à 8 dans une séquence de mots de code de 15 bits en réponse à un signal de commande en provenance desdits moyens de commande (1);
dans lequel lesdits moyens de conversion (2 - 7) produisent une multiplicité de premières paires de codes comprenant chacune un mot de code de 15 bits ayant une somme numérique de mot de code de +3 et un mot de code de 15 bits ayant une somme numérique de mot de code de -1, et une multiplicité de secondes paires de codes comprenant chacune un mot de code de 15 bits ayant une somme numérique de mot de code de +1 et un mot de code de 15 bits ayant une somme numérique de mot de code de -3, affectent une paire de ladite multiplicité de premières paires de codes et une paire de ladite multiplicité de secondes paires de codes à chaque mot de données de 8 bits, sélectionnent l'une des première et seconde paires de codes affectées à chaque mot de données de 8 bits de sorte que le nombre de bits identiques consécutifs ne soit pas inférieur à 2 et ne soit pas supérieur à 8 dans une séquence de mots de code de 15 bits, et sélectionnent l'un de deux mots de code de 15 bits compris dans la paire de codes sélectionnée de sorte que la variation de somme numérique au niveau d'un dernier bit de chaque mot de code de 15 bits varie pé-

riodiquement.

10. Appareil de modulation numérique selon la revendication 9, dans lequel:

ledit signal de commande représente une différence entre une valeur de contrôle de variation de somme numérique au niveau d'un dernier bit d'un mot de code de 15 bits courant et une valeur de contrôle de variation de somme numérique au niveau d'un dernier bit d'un mot de code de 15 bits suivant, et ladite valeur de contrôle de variation de somme numérique représente une valeur cible de variation de somme numérique qui change périodiquement; et
lesdits moyens de conversion (2 - 7) convertissent chaque mot de données de 8 bits en un mot de code de 15 bits sur la base d'une différence entre une valeur de contrôle de variation de somme numérique au niveau d'un dernier bit d'un mot de code de 15 bits courant et une valeur réelle de variation de somme numérique au niveau d'un dernier bit d'un mot de code de 15 bits courant.

11. Appareil de modulation numérique selon la revendication 10, dans lequel lesdits moyens de conversion comportent:

des premiers moyens d'addition (2);
des premiers moyens de maintien (3) pour maintenir temporairement une sortie desdits premiers moyens d'addition (2);
des seconds moyens d'addition (4);
des moyens de génération de signal (5) pour générer un signal de sélection en réponse à une sortie desdits seconds moyens d'addition (4);
des moyens de conversion 8-15 (6);
des moyens de sortie (6) pour délivrer une différence entre une valeur réelle de variation de somme numérique au niveau d'un dernier bit d'un mot de code de 15 bits suivant et une valeur réelle de variation de somme numérique au niveau d'un dernier bit d'un mot de code de 15 bits courant; et
des seconds moyens de maintien (7) pour maintenir temporairement les deux derniers bits d'un mot de code de 15 bits, dans lequel:
lesdits premiers moyens d'addition (2) additionnent une sortie desdits moyens de commande (1), une sortie desdits premiers moyens de maintien (3) et une sortie desdits moyens de sortie (6);
lesdits seconds moyens d'addition (4) additionnent une sortie desdits moyens de commande (1) et une sortie desdits premiers moyens de maintien (3); et
lesdits moyens de conversion 8-15 (6) sélectionnent et délivrent l'un desdits mots de code de 15 bits sur la base d'un mot de données de 8 bits introduit, dudit signal de sélection et d'une sortie desdits seconds moyens de maintien (7).

12. Appareil de modulation numérique selon la revendication 11, dans lequel:

lesdits moyens de génération de signal (5) génèrent un premier signal de commande lorsqu'une sortie desdits seconds moyens d'addition (4) constitue une première valeur, génèrent un second signal de commande lorsqu'une sortie desdits seconds moyens d'addition (4) constitue une seconde valeur, et génèrent un troisième signal de commande lorsqu'une sortie desdits seconds moyens d'addition (4) constitue une troisième valeur; et
lesdits moyens de conversion 8-15 (6) sélectionnent un mot de code de 15 bits ayant une somme numérique de mot de code de -1 ou -3 en réponse audit premier signal de sélection, sélectionnent un mot de code de 15 bits ayant une somme numérique de mot de code de +1 ou -1 en réponse audit second signal de commande, et sélectionnent un mot de code de 15 bits ayant une somme numérique de mot de code de +3 ou +1 en réponse audit troisième signal de commande.

13. Appareil de modulation numérique selon la revendication 11, comportant en outre des moyens de conversion parallèle/série (8) pour convertir un mot de code de 15 bits délivré par lesdits moyens de conversion 8-15 (6) en un signal modulé de données série de 15 bits.

FIG. 1

FIRST 2 BITS	CDS	NUMBER OF CORRESPONDING CODEWORDS
00	+3	54
	+1	95
	-1	120
	-3	115
01	+3	65
	+1	79
	-1	71
	-3	47
10	+3	47
	+1	71
	-1	79
	-3	65
11	+3	115
	+1	120
	-1	95
	-3	54

FIG. 2

FIRST 2 BITS	CODE PAIR	NUMBER	8-BIT DATA WORDS TO BE CORRESPONDED	USED NUMBER
00	+3, -1	54	0 ~ 52	53
	+1, -3	95	53 ~ 146	94
01	+3, -1	65	147 ~ 210	64
	+1, -3	47	211 ~ 255	45
10	+3, -1	47	211 ~ 255	45
	+1, -3	65	147 ~ 210	64
11	+3, -1	95	53 ~ 146	94
	+1, -3	54	0 ~ 52	53

FIG. 3A

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
00	000011001111111	+3	0000000111111110	-1	110000000111111	+1	110000000011110	-3
01	000011100111111	+3	0000000110011111	-1	110000001111110	+1	110000000110011	-3
02	000011110011111	+3	0000000111001111	-1	110000011001111	+1	110000000111001	-3
03	000011111001111	+3	0000000111100111	-1	110000011100111	+1	110000000111100	-3
04	000011111100111	+3	0000000111110011	-1	110000011110011	+1	110000001100011	-3
05	000011111110011	+3	0000000111111001	-1	110000011111001	+1	110000001100110	-3
06	000011111111001	+3	0000000111111100	-1	110000011111100	+1	110000001110001	-3
07	000110001111111	+3	0000001100011111	-1	110000110001111	+1	110000001111000	-3
08	000110011111110	+3	0000001100111110	-1	110000110011110	+1	110000011000011	-3
09	000111000111111	+3	0000001110001111	-1	110000111000111	+1	110000011000110	-3
0A	000111001111110	+3	0000001110011110	-1	110000111001110	+1	110000011001100	-3
0B	000111100011111	+3	0000001111000111	-1	110000111100011	+1	110000011100001	-3
0C	000111100111110	+3	0000001111001110	-1	110000111100110	+1	110000011110000	-3
0D	000111110001111	+3	0000001111100011	-1	110000111110001	+1	110000110000011	-3
0E	000111110011110	+3	0000001111100110	-1	110000111111000	+1	110000110000110	-3
0F	000111111000111	+3	0000001111110001	-1	110001100001111	+1	110000110001100	-3

FIG. 3B

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
10	000111111001110	+3	0000011111111000	-1	1100011000111110	+1	1100000110011000	-3
11	000111111100011	+3	0000110000111111	-1	1100011001100111	+1	1100000111000001	-3
12	000111111100110	+3	0000110001111110	-1	1100011001110011	+1	1100000111100000	-3
13	000111111110001	+3	0000110011001111	-1	1100011001111100	+1	1100011000000011	-3
14	001100001111111	+3	0000110011100111	-1	1100011100000111	+1	1100011000000110	-3
15	001100011111110	+3	0000110011111001	-1	1100011100001110	+1	1100011000001100	-3
16	001100110011111	+3	0000110011111100	-1	1100011100011001	+1	1100011000011000	-3
17	001100111001111	+3	0000111000011111	-1	1100011100111100	+1	1100011001100000	-3
18	001100111100111	+3	0000111000111110	-1	1100011110000011	+1	1100011100000001	-3
19	001100111110011	+3	0000111001100111	-1	1100011110000110	+1	1100011110000000	-3
1A	001100111111001	+3	0000111001111001	-1	1100011110011100	+1	1100110000000011	-3
1B	001100111111100	+3	0000111001111100	-1	1100011111100001	+1	1100110000000110	-3
1C	001110000111111	+3	0000111110000111	-1	1100011111110000	+1	1100110000001100	-3
1D	001110001111110	+3	0000111110001110	-1	1100110000011111	+1	1100110000011000	-3
1E	001110011001111	+3	0000111110011001	-1	1100110000111110	+1	1100110001100000	-3
1F	001110011100111	+3	0000111110011100	-1	1100110001100111	+1	1100110011000000	-3

FIG. 4A

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
20	001110011110011	+3	000011111000011	-1	110011000111001	+1	110011100000001	-3
21	001110011111001	+3	000011111000110	-1	110011000111100	+1	110011110000000	-3
22	001110011111100	+3	000011111001100	-1	110011001100011	+1	111000000001110	-3
23	001111000011111	+3	000011111100001	-1	110011001100110	+1	111000000011001	-3
24	001111000111110	+3	000011111110000	-1	110011001110001	+1	111000000011100	-3
25	001111001100111	+3	000110000011111	-1	110011001111000	+1	111000000110001	-3
26	001111001110011	+3	000110000111110	-1	110011100000111	+1	111000000111000	-3
27	001111001111001	+3	000110001100111	-1	110011100001110	+1	111000001100001	-3
28	001111001111100	+3	000110001110011	-1	110011100011001	+1	111000001110000	-3
29	001111100001111	+3	000110001111001	-1	110011100011100	+1	111000011000001	-3
2A	001111100011110	+3	000110001111100	-1	110011100110001	+1	111000011100000	-3
2B	001111100110011	+3	000110011000111	-1	110011100111000	+1	111000110000001	-3
2C	001111100111001	+3	000110011001110	-1	110011110000011	+1	111000111000000	-3
2D	001111100111100	+3	000110011100011	-1	110011110000110	+1	111001100000001	-3
2E	001111110000111	+3	000110011100110	-1	110011110001100	+1	111001110000000	-3
2F	001111110001110	+3	000110011110001	-1	110011110011000	+1	111100000000110	-3

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FIG. 4B

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
30	001111110011001	+3	0001100111111000	-1	110011111000001	+1	111100000001100	-3
31	001111110011100	+3	0001111000001111	-1	110011111100000	+1	111100000011000	-3
32	001111111000011	+3	0001111000011110	-1	111000000011111	+1	111100000110000	-3
33	001111111000110	+3	0001111000110011	-1	111000000111110	+1	111100001100000	-3
34	001111111001100	+3	0001111000111001	-1	111000001100111	+1	111100011000000	-3
35	0000001111111110	+1	0000000110011111	-3	110000001111111	+3	110000000011111	-1
36	0000011001111111	+1	0000000111001111	-3	110000011111110	+3	110000000111110	-1
37	0000011100111111	+1	0000000111110011	-3	110000110011111	+3	110000001100111	-1
38	0000011110011111	+1	0000000111111001	-3	110000111001111	+3	110000001110011	-1
39	0000011111100111	+1	0000000111111100	-3	110000111100111	+3	110000001111001	-1
3A	0000011111110011	+1	0000000110001111	-3	110000111110011	+3	110000001111100	-1
3B	0000011111111001	+1	0000000110011110	-3	110000111111001	+3	110000011000111	-1
3C	0000011111111100	+1	0000000111000111	-3	110000111111100	+3	110000011001110	-1
3D	0000011000111111	+1	0000000111001110	-3	110001100011111	+3	110000011100011	-1
3E	0000011001111110	+1	0000000111100011	-3	110001100111110	+3	110000011100110	-1
3F	0000011100011111	+1	0000000111100110	-3	110001110001111	+3	110000011110001	-1

FIG. 5A

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
40	000011100111110	+1	000000111110001	-3	110001110011110	+3	110000011111000	-1
41	000011110001111	+1	000000111111000	-3	110001111000111	+3	110000110000111	-1
42	000011110011110	+1	000001100001111	-3	110001111001110	+3	110000110001110	-1
43	000011111000111	+1	000001100011110	-3	110001111100011	+3	110000110011001	-1
44	000011111001110	+1	000001100110011	-3	110001111100110	+3	110000110011100	-1
45	000011111100011	+1	000001100111001	-3	110001111110001	+3	110000111000011	-1
46	000011111100110	+1	000001100111100	-3	110001111111000	+3	110000111000110	-1
47	000011111110001	+1	000001110000111	-3	110011000011111	+3	110000111001100	-1
48	000011111111000	+1	000001110001110	-3	110011000111110	+3	110000111100001	-1
49	000110000111111	+1	000001110011001	-3	110011001100111	+3	110000111110000	-1
4A	000110001111110	+1	000001110011100	-3	110011001110011	+3	110001100000111	-1
4B	000110011001111	+1	000001111000011	-3	110011001111001	+3	110001100001110	-1
4C	000110011100111	+1	000001111000110	-3	110011001111100	+3	110001100011001	-1
4D	000110011110011	+1	000001111001100	-3	110011100001111	+3	110001100011100	-1
4E	000110011111001	+1	000001111100001	-3	110011100011110	+3	110001100110001	-1
4F	000110011111100	+1	000001111110000	-3	110011100110011	+3	110001100111000	-1

FIG. 5B

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
50	000111000011111	+1	000011000001111	-3	110011100111001	+3	110001110000011	-1
51	000111000111110	+1	000011000011110	-3	110011100111100	+3	110001110000110	-1
52	000111001100111	+1	000011000110011	-3	110011110000111	+3	110001110001100	-1
53	000111001110011	+1	000011000111001	-3	110011110001110	+3	110001110011000	-1
54	000111001111001	+1	000011000111100	-3	110011110011001	+3	110001111000001	-1
55	000111001111100	+1	000011001100011	-3	110011110011100	+3	110001111100000	-1
56	000111100001111	+1	000011001100110	-3	110011111000011	+3	110011000000111	-1
57	000111100011110	+1	000011001110001	-3	110011111000110	+3	110011000001110	-1
58	000111100110011	+1	000011001111000	-3	110011111001100	+3	110011000011001	-1
59	000111100111001	+1	000011100000111	-3	110011111100001	+3	110011000011100	-1
5A	000111100111100	+1	000011100001110	-3	110011111110000	+3	110011000110001	-1
5B	000111110000111	+1	000011100011001	-3	111000000111111	+3	110011000111000	-1
5C	000111110001110	+1	000011100011100	-3	111000001111110	+3	110011001100001	-1
5D	000111110011001	+1	000011100110001	-3	111000011001111	+3	110011001110000	-1
5E	000111110011100	+1	000011100111000	-3	111000011100111	+3	110011100000011	-1
5F	000111111000011	+1	000011110000011	-3	111000011110011	+3	110011100000110	-1

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FIG. 6A

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
60	000111111000110	+1	000011110000110	-3	111000011111001	+3	110011100001100	-1
61	000111111001100	+1	000011110001100	-3	111000011111100	+3	110011100011000	-1
62	000111111100001	+1	000011110011000	-3	111000110001111	+3	110011100110000	-1
63	000111111110000	+1	000011111000001	-3	111000110011110	+3	110011110000001	-1
64	001100000111111	+1	000011111100000	-3	111000111000111	+3	110011111000000	-1
65	001100001111110	+1	000110000001111	-3	111000111001110	+3	111000000001111	-1
66	001100011001111	+1	000110000011110	-3	111000111100011	+3	111000000011110	-1
67	001100011100111	+1	000110000110011	-3	111000111100110	+3	111000000110011	-1
68	001100011110011	+1	000110000111001	-3	111000111110001	+3	111000000111001	-1
69	001100011111001	+1	000110000111100	-3	111000111111000	+3	111000000111100	-1
6A	001100011111100	+1	000110001100011	-3	111001100001111	+3	111000001100011	-1
6B	001100110001111	+1	000110001100110	-3	111001100011110	+3	111000001100110	-1
6C	001100110011110	+1	000110001110001	-3	111001100110011	+3	111000001110001	-1
6D	001100111000111	+1	000110001111000	-3	111001100111001	+3	111000001111000	-1
6E	001100111001110	+1	000110011000011	-3	111001100111100	+3	111000011000011	-1
6F	001100111100011	+1	000110011000110	-3	111001110000111	+3	111000011000110	-1

FIG. 6B

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
70	0011001111100110	+1	0001100110011100	-3	1110011100011110	+3	1110000110011100	-1
71	0011001111110001	+1	0001100111100001	-3	1110011100111001	+3	1110000111100001	-1
72	0011001111111000	+1	0001100111110000	-3	1110011100111100	+3	1110000111110000	-1
73	0011100000111111	+1	0001110000000111	-3	1110011110000011	+3	1110001100000011	-1
74	0011100000111110	+1	0001110000001110	-3	1110011110000110	+3	1110001100000110	-1
75	0011100011100111	+1	0001110000011001	-3	1110011110011100	+3	1110001100011100	-1
76	0011100011110011	+1	0001110000011100	-3	1110011111100001	+3	1110001100111000	-1
77	0011100011111001	+1	0001110001100001	-3	1110011111110000	+3	1110001111000001	-1
78	0011100011111100	+1	0001110001111000	-3	1111000000111111	+3	1110001111100000	-1
79	0011100110000111	+1	0001110011100001	-3	1111000001111110	+3	1110011000000011	-1
7A	0011100110011110	+1	0001110011110000	-3	1111000011001111	+3	1110011000000110	-1
7B	0011100111000011	+1	0001111000000011	-3	1111000011100111	+3	1110011000011100	-1
7C	0011100111001110	+1	0001111000000110	-3	1111000011111001	+3	1110011000111000	-1
7D	0011100111110001	+1	0001111000011100	-3	1111000011111100	+3	1110011001100000	-1
7E	0011100111111000	+1	0001111000111000	-3	1111000110001111	+3	1110011100000001	-1
7F	0011111000001111	+1	0001111001100000	-3	1111000110011110	+3	1110011111000000	-1

FIG. 7A

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
80	001111000011110	+1	000111110000001	-3	111100011100011	+3	111100000000111	-1
81	001111000110011	+1	000111111000000	-3	111100011100110	+3	111100000001110	-1
82	001111000111001	+1	001100000001111	-3	111100011110001	+3	111100000011001	-1
83	001111000111100	+1	001100000011110	-3	111100011111000	+3	111100000011100	-1
84	001111001100011	+1	001100000110011	-3	111100110000111	+3	111100000110001	-1
85	001111001100110	+1	001100000111001	-3	111100110001110	+3	111100000111000	-1
86	001111001110001	+1	001100000111100	-3	111100110011001	+3	111100001100001	-1
87	001111001111000	+1	001100001100011	-3	111100110011100	+3	111100001110000	-1
88	001111100000111	+1	001100001100110	-3	111100111000011	+3	111100011000001	-1
89	001111100001110	+1	001100001110001	-3	111100111000110	+3	111100011100000	-1
8A	001111100011001	+1	001100001111000	-3	111100111001100	+3	111100110000001	-1
8B	001111100011100	+1	001100011000011	-3	111100111100001	+3	111100111000000	-1
8C	001111100110001	+1	001100011000110	-3	111100111110000	+3	111110000000011	-1
8D	001111100111000	+1	001100011001100	-3	111110000001111	+3	111110000000110	-1
8E	001111110000011	+1	001100011100001	-3	111110000011110	+3	111110000001100	-1
8F	001111110000110	+1	001100011110000	-3	111110000110011	+3	111110000011000	-1

FIG. 7B

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
90	001111110001100	+1	001100110000011	-3	111110000111001	+3	111110000110000	-1
91	001111110011000	+1	001100110000110	-3	111110000111100	+3	111110001100000	-1
92	001111111000001	+1	001100110001100	-3	111110001100011	+3	111110011000000	-1
93	011000001111111	+3	011000000011111	-1	100000001111111	+1	100000000111110	-3
94	011000011111110	+3	011000000111110	-1	100000011111110	+1	100000001100111	-3
95	011000110011111	+3	011000001100111	-1	100000110011111	+1	100000001110011	-3
96	011000111001111	+3	011000001110011	-1	100000111001111	+1	100000001111001	-3
97	011000111100111	+3	011000001111001	-1	100000111100111	+1	100000001111100	-3
98	011000111110011	+3	011000001111100	-1	100000111110011	+1	100000011000111	-3
99	011000111111001	+3	011000011000111	-1	100000111111001	+1	100000011001110	-3
9A	011000111111100	+3	011000011001110	-1	100000111111100	+1	100000011100011	-3
9B	011001100011111	+3	011000011100011	-1	100001100011111	+1	100000011100110	-3
9C	011001100111110	+3	011000011100110	-1	100001100111110	+1	100000011110001	-3
9D	011001110001111	+3	011000011110001	-1	100001110001111	+1	100000011111000	-3
9E	011001110011110	+3	011000011111000	-1	100001110011110	+1	100000110000111	-3
9F	011001111000111	+3	011000110000111	-1	100001111000111	+1	100000110001110	-3

FIG. 8A

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
A0	011001111001110	+3	011000110001110	-1	100001111001110	+1	100000110011001	-3
A1	011001111100011	+3	011000110011001	-1	100001111100011	+1	100000110011100	-3
A2	011001111100110	+3	011000110011100	-1	100001111100110	+1	100000111000011	-3
A3	011001111110001	+3	011000111000011	-1	100001111110001	+1	100000111000110	-3
A4	011001111111000	+3	011000111000110	-1	100001111111000	+1	100000111001100	-3
A5	011100000111111	+3	011000111001100	-1	100011000011111	+1	100000111100001	-3
A6	011100001111110	+3	011000111100001	-1	100011000111110	+1	100000111110000	-3
A7	011100011001111	+3	011000111110000	-1	100011001100111	+1	100001100000111	-3
A8	011100011100111	+3	011001100000111	-1	100011001110011	+1	100001100001110	-3
A9	011100011110011	+3	011001100001110	-1	100011001111001	+1	100001100011001	-3
AA	011100011111001	+3	011001100011001	-1	100011001111100	+1	100001100011100	-3
AB	011100011111100	+3	011001100011100	-1	100011100001111	+1	100001100110001	-3
AC	011100110001111	+3	011001100110001	-1	100011100011110	+1	100001100111000	-3
AD	011100110011110	+3	011001100111000	-1	100011100110011	+1	100001110000011	-3
AE	011100111000111	+3	011001110000011	-1	100011100111001	+1	100001110000110	-3
AF	011100111001110	+3	011001110000110	-1	100011100111100	+1	100001110001100	-3

FIG. 8B

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
B0	011100111100011	+3	011001110001100	-1	100011110000111	+1	100001110011000	-3
B1	011100111100110	+3	011001110011000	-1	100011110001110	+1	100001111000001	-3
B2	011100111110001	+3	011001111000001	-1	100011110011001	+1	100001111100000	-3
B3	011100111111000	+3	011001111100000	-1	100011110011100	+1	100011000000111	-3
B4	011110000011111	+3	011100000001111	-1	100011111000011	+1	100011000001110	-3
B5	011110000111110	+3	011100000011110	-1	100011111000110	+1	100011000011001	-3
B6	011110001100111	+3	011100000110011	-1	100011111001100	+1	100011000011100	-3
B7	011110001110011	+3	011100000111001	-1	100011111100001	+1	100011000110001	-3
B8	011110001111001	+3	011100000111100	-1	100011111110000	+1	100011000111000	-3
B9	011110001111100	+3	011100001100011	-1	100110000011111	+1	100011001100001	-3
BA	011110011000111	+3	011100001100110	-1	100110000111110	+1	100011001110000	-3
BB	011110011001110	+3	011100001110001	-1	100110001100111	+1	100011100000011	-3
BC	011110011100011	+3	011100001111000	-1	100110001110011	+1	100011100000110	-3
BD	011110011100110	+3	011100011000011	-1	100110001111001	+1	100011100001100	-3
BE	011110011110001	+3	011100011000110	-1	100110001111100	+1	100011100011000	-3
BF	011110011111000	+3	011100011001100	-1	100110011000111	+1	100011100110000	-3

FIG. 9A

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
C0	011111000001111	+3	011100011100001	-1	100110011001110	+1	100011110000001	-3
C1	011111000011110	+3	011100011110000	-1	100110011100011	+1	100011111000000	-3
C2	011111000110011	+3	011100110000011	-1	100110011100110	+1	100110000000111	-3
C3	011111000111001	+3	011100110000110	-1	100110011110001	+1	100110000001110	-3
C4	011111000111100	+3	011100110001100	-1	100110011111000	+1	100110000011001	-3
C5	011111001100011	+3	011100110011000	-1	100111000001111	+1	100110000011100	-3
C6	011111001100110	+3	011100111000001	-1	100111000011110	+1	100110000110001	-3
C7	011111001110001	+3	011100111100000	-1	100111000110011	+1	100110000111000	-3
C8	011111001111000	+3	011110000000111	-1	100111000111001	+1	100110001100001	-3
C9	011111100000111	+3	011110000001110	-1	100111000111100	+1	100110001110000	-3
CA	011111100001110	+3	011110000011001	-1	100111001100011	+1	100110011000001	-3
CB	011111100011001	+3	011110000011100	-1	100111001100110	+1	100110011100000	-3
CC	011111100011100	+3	011110000110001	-1	100111001110001	+1	100111000000011	-3
CD	011111100110001	+3	011110000111000	-1	100111001111000	+1	100111000000110	-3
CE	011111100111000	+3	011110001100001	-1	100111100000111	+1	100111000001100	-3
CF	011111110000011	+3	011110001110000	-1	100111100001110	+1	100111000011000	-3

FIG. 9B

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
D0	011111110000110	+3	011110011000001	-1	100111100011001	+1	100111000110000	-3
D1	011111110001100	+3	011110011100000	-1	100111100011100	+1	100111001100000	-3
D2	011111110011000	+3	011111000000011	-1	100111100110001	+1	100111100000001	-3
D3	011000000111111	+1	011000000001111	-3	100000111111110	+3	100000000111111	-1
D4	011000001111110	+1	011000000011110	-3	100001100111111	+3	100000001111110	-1
D5	011000011001111	+1	011000000110011	-3	100001110011111	+3	100000011001111	-1
D6	011000011100111	+1	011000000111001	-3	100001111001111	+3	100000011100111	-1
D7	011000011110011	+1	011000000111100	-3	100001111100111	+3	100000011110011	-1
D8	011000011111001	+1	011000001100011	-3	100001111110011	+3	100000011111001	-1
D9	011000011111100	+1	011000001100110	-3	100001111111001	+3	100000011111100	-1
DA	011000110001111	+1	011000001110001	-3	100001111111100	+3	100000110001111	-1
DB	011000110011110	+1	011000001111000	-3	100011000111111	+3	100000110011110	-1
DC	011000111000111	+1	011000011000011	-3	100011001111110	+3	100000111000111	-1
DD	011000111001110	+1	011000011000110	-3	100011100011111	+3	100000111001110	-1
DE	011000111100011	+1	011000011001100	-3	100011100111110	+3	100000111100011	-1
DF	011000111100110	+1	011000011100001	-3	100011110001111	+3	100000111100110	-1

FIG. 10A

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
E0	011000111110001	+1	011000011110000	-3	100011110011110	+3	100000111110001	-1
E1	011000111111000	+1	011000110000011	-3	100011111000111	+3	100000111111000	-1
E2	011001100001111	+1	011000110000110	-3	100011111001110	+3	100001100001111	-1
E3	011001100011110	+1	011000110001100	-3	100011111100011	+3	100001100011110	-1
E4	011001100110011	+1	011000110011000	-3	100011111100110	+3	100001100110011	-1
E5	011001100111001	+1	011000111000001	-3	100011111110001	+3	100001100111001	-1
E6	011001100111100	+1	011000111100000	-3	100011111111000	+3	100001100111100	-1
E7	011001110000111	+1	011001100000011	-3	100110000111111	+3	100001110000111	-1
E8	011001110001110	+1	011001100000110	-3	100110001111110	+3	100001110001110	-1
E9	011001110011001	+1	011001100001100	-3	100110011001111	+3	100001110011001	-1
EA	011001110011100	+1	011001100011000	-3	100110011100111	+3	100001110011100	-1
EB	011001111000011	+1	011001100110000	-3	100110011110011	+3	100001111000011	-1
EC	011001111000110	+1	011001110000001	-3	100110011111001	+3	100001111000110	-1
ED	011001111001100	+1	011001111000000	-3	100110011111100	+3	100001111001100	-1
EE	011001111100001	+1	011100000000111	-3	100111000011111	+3	100001111100001	-1
EF	011001111110000	+1	011100000001110	-3	100111000111110	+3	100001111110000	-1

EP 0 506 446 B1

FIG. 10B

8-BIT DATA WORD (HEX)	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS	CODEWORD	CDS
F0	011100000011111	+1	011100000011001	-3	100111001100111	+3	100011000001111	-1
F1	011100000111110	+1	011100000011100	-3	100111001110011	+3	100011000011110	-1
F2	011100001100111	+1	011100000110001	-3	100111001111001	+3	100011000110011	-1
F3	011100001110011	+1	011100000111000	-3	100111001111100	+3	100011000111001	-1
F4	011100001111001	+1	011100001100001	-3	100111100001111	+3	100011000111100	-1
F5	011100001111100	+1	011100001110000	-3	100111100011110	+3	100011001100011	-1
F6	011100011000111	+1	011100011000001	-3	100111100110011	+3	100011001100110	-1
F7	011100011001110	+1	011100011100000	-3	100111100111001	+3	100011001110001	-1
F8	011100011100011	+1	011100110000001	-3	100111100111100	+3	100011001111000	-1
F9	011100011100110	+1	011100111000000	-3	100111110000111	+3	100011100000111	-1
FA	011100011110001	+1	011110000000011	-3	100111110001110	+3	100011100001110	-1
FB	011100011111000	+1	011110000000110	-3	100111110011001	+3	100011100011001	-1
FC	011100110000111	+1	011110000001100	-3	100111110011100	+3	100011100011100	-1
FD	011100110001110	+1	011110000011000	-3	100111111000011	+3	100011100110001	-1
FE	011100110011001	+1	011110000110000	-3	100111111000110	+3	100011100111000	-1
FF	011100110011100	+1	011110001100000	-3	100111111001100	+3	100011110000011	-1

FIG.11

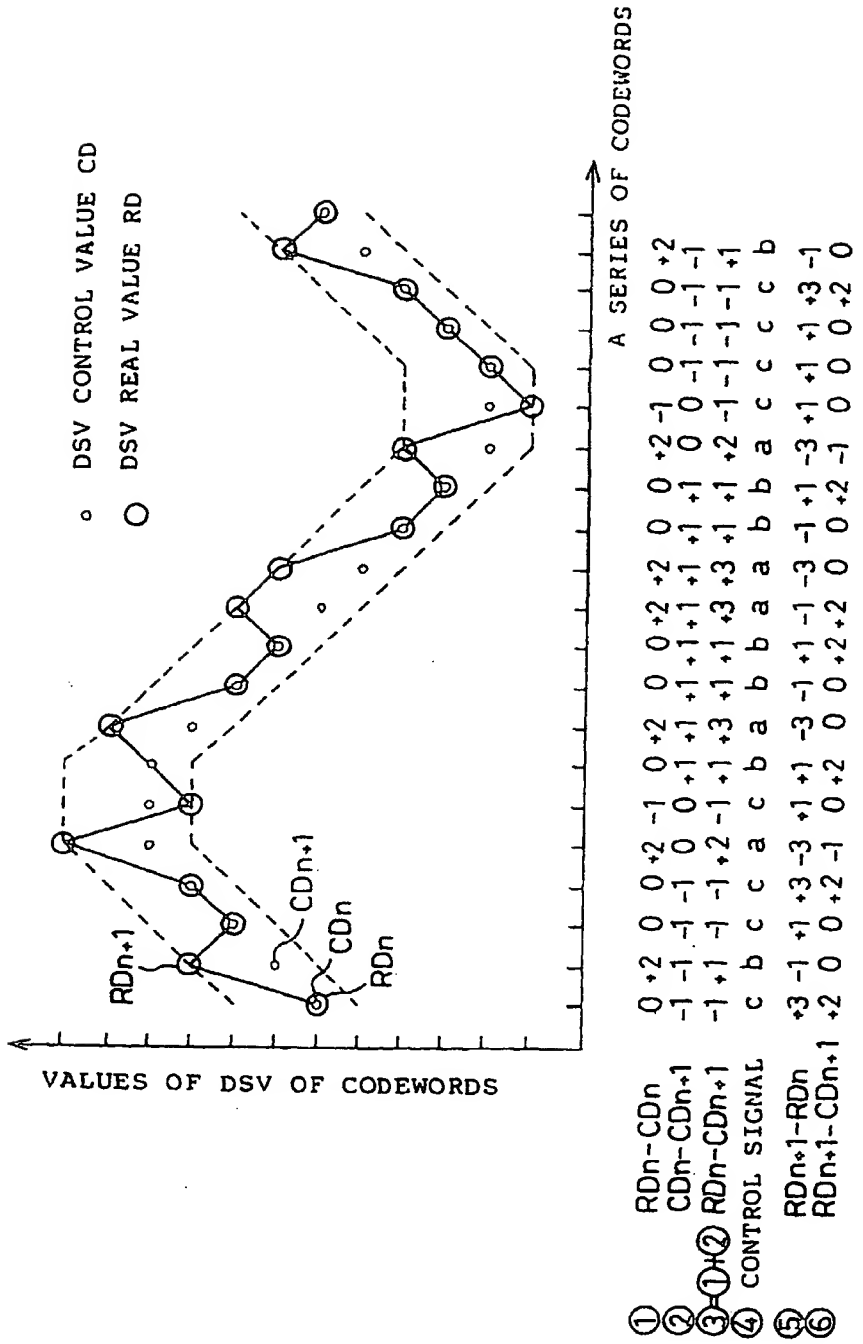
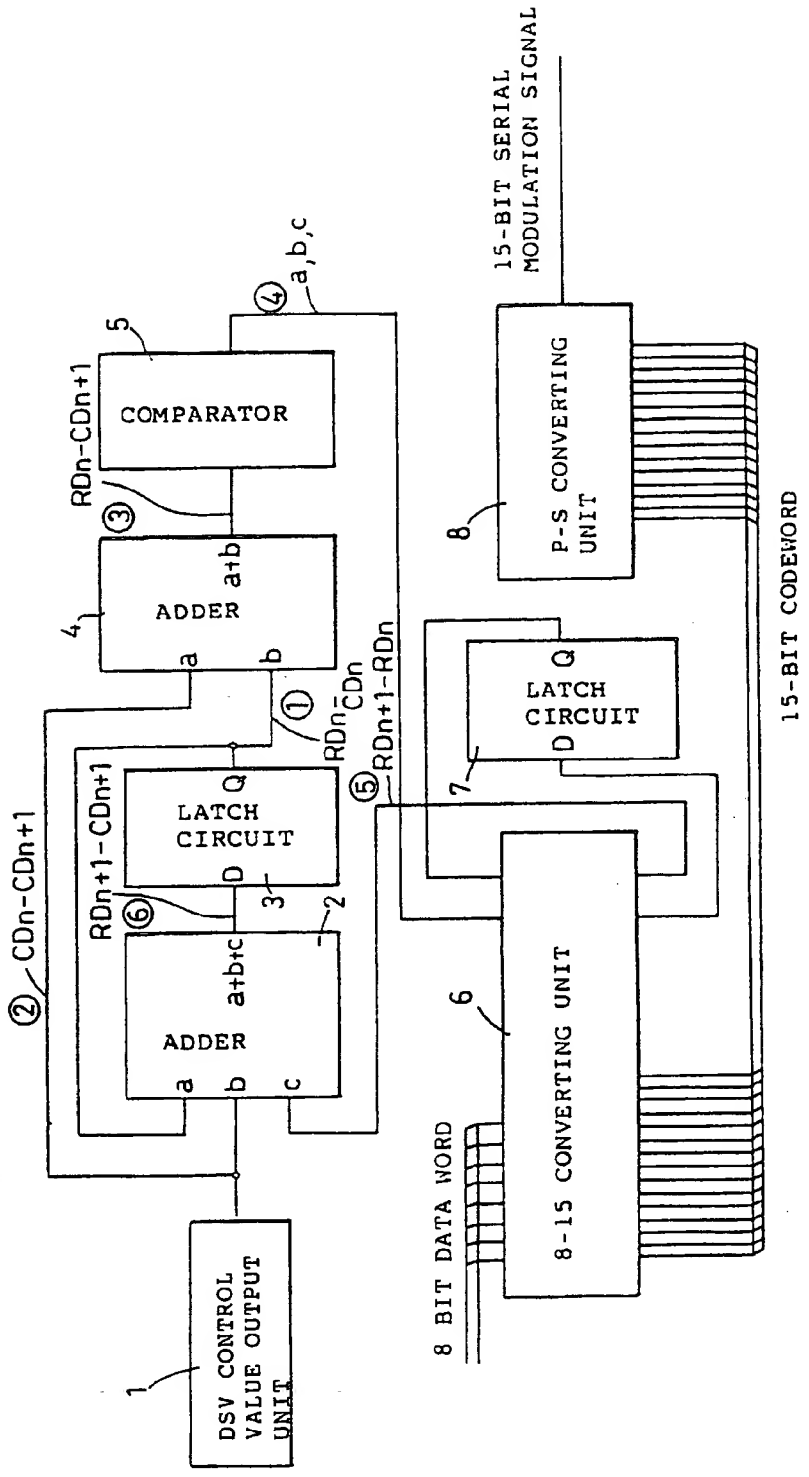

DSV CONTROL VALUE CD
DSV REAL VALUE RD
VALUES OF DSV OF CODEWORDS
A SERIES OF CODEWORDS
RDn+1
CDn+1
CDn
RDn
RDn-CDn 0 +2 0 0 +2 -1 0 +2 0 0 +2 +2 0 0 +2 -1 0 0 0 +2
CDn-CDn+1 -1 -1 -1 -1 0 0 +1 +1 +1 +1 +1 +1 +1 0 0 -1 -1 -1 -1
RDn-CDn+1 -1 +1 -1 -1 +2 -1 +1 +3 +1 +1 +3 +3 +1 +1 +2 -1 -1 -1 -1 +1
CONTROL SIGNAL c b c c a c b a b b a a b b a c c c c b
RDn+1-RDn +3 -1 +1 +3 -3 +1 +1 -3 -1 +1 -1 -3 -1 +1 -3 +1 +1 +1 +3 -1
RDn+1-CDn+1 +2 0 0 +2 -1 0 +2 0 0 +2 +2 0 0 +2 -1 0 0 0 +2 0
① ② ③ ④ ⑤ ⑥

FIG. 12

RDn-CDn	CDn-CDn+1	CODE PAIR (+1,-3) +1	CODE PAIR (+1,-3) -3	CODE PAIR(+3,-1) +3	CODE PAIR(+3,-1) -1
+2	+1		O		O
	0		O		O
	-1	O			O
+1	+1		O		O
	0	O			O
	-1	O			
0	+1	O		O	O
	0	O			
	-1	O			
-1	+1	O		O	O
	0	O			
	-1	O			

FIG.13


DSV CONTROL VALUE OUTPUT UNIT
1
CDn-CDn+1
RDn+1-CDn+1
RDn+1-RDn
RDn-CDn+1
a,b,c
COMPARATOR
5
ADDER
a+b
a
b
4
ADDER
a+b+c
a
b
c
LATCH CIRCUIT
D
Q
LATCH CIRCUIT
D
Q
RDn
CDn
2
3
6
7
8-15 CONVERTING UNIT
6
8 BIT DATA WORD
P-S CONVERTING UNIT
8
15-BIT SERIAL MODULATION SIGNAL
15-BIT CODEWORD

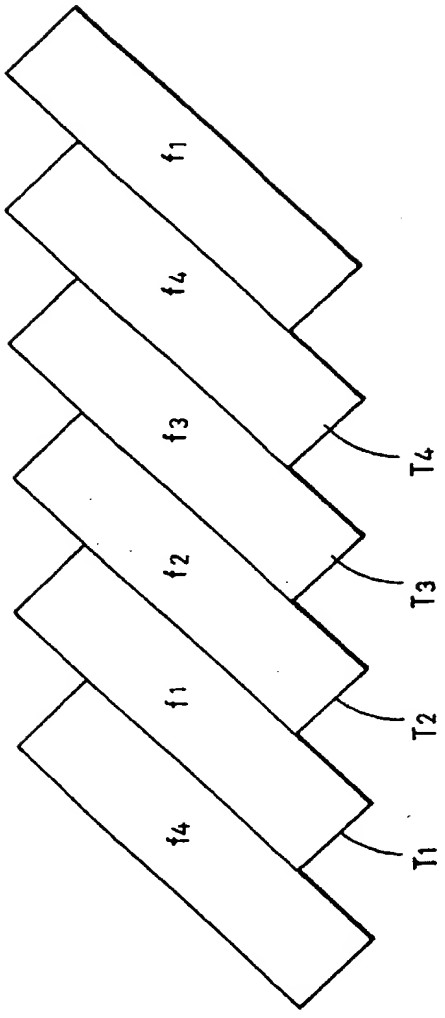
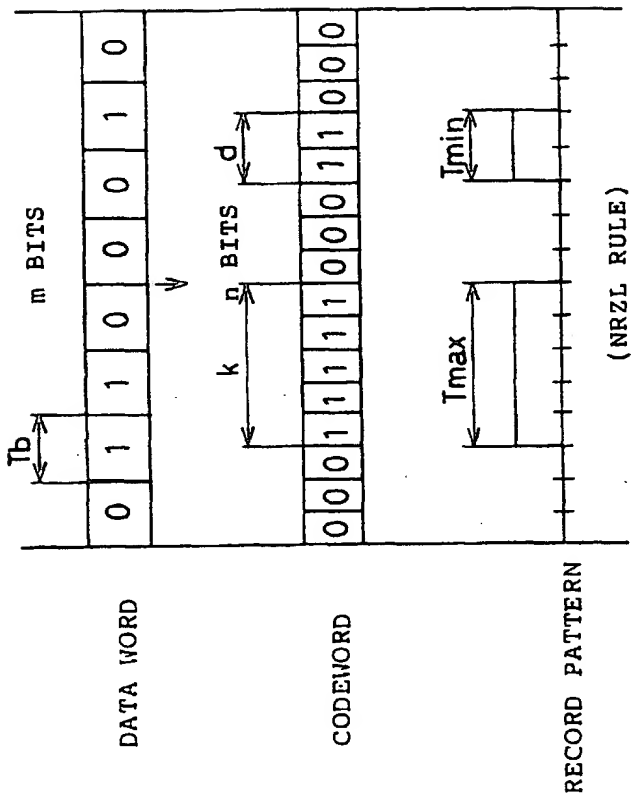


FIG. 14

FIG.15


m BITS
n BITS
Tb
k
d
Tmax
Tmin
(NRZI RULE)
DATA WORD
CODEWORD
RECORD PATTERN